

## TPS3710 Wide VIN Voltage Detector

### 1 Features

- Wide Supply Voltage Range: 1.8 V to 18 V
- Adjustable Threshold: Down to 400 mV
- High Threshold Accuracy:
  - 1.0% Over Temperature
  - 0.25% (Typical)
- Low Quiescent Current: 5.5  $\mu$ A (Typical)
- Open-Drain Output
- Internal Hysteresis: 5.5 mV (Typical)
- Temperature Range:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Packages:
  - SOT-6
  - 1.5-mm  $\times$  1.5-mm WSON-6

### 2 Applications

- Industrial Control Systems
- Automotive Systems
- Embedded Computing Modules
- DSP, Microcontroller, or Microprocessor Applications
- Notebook and Desktop Computers
- Portable- and Battery-Powered Products
- FPGA and ASIC Applications

### 3 Description

The TPS3710 wide-supply voltage detector operates over a 1.8-V to 18-V range. The device has a high-accuracy comparator with an internal 400-mV reference and an open-drain output rated to 18 V for precision voltage detection. The monitored voltage can be set with the use of external resistors.

The OUT pin is driven low when the voltage at the SENSE pin drops below ( $V_{IT-}$ ), and goes high when the voltage returns above the respective threshold ( $V_{IT+}$ ). The comparator in the TPS3710 includes built-in hysteresis for filtering to reject brief glitches, thereby ensuring stable output operation without false triggering.

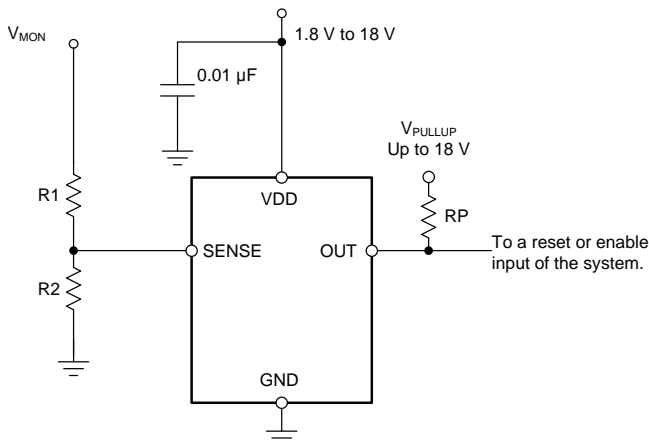
The TPS3710 is available in a SOT-6 package, and a 1.5-mm  $\times$  1.5-mm WSON-6 package, and is specified over the junction temperature range of  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

#### Device Information (1)

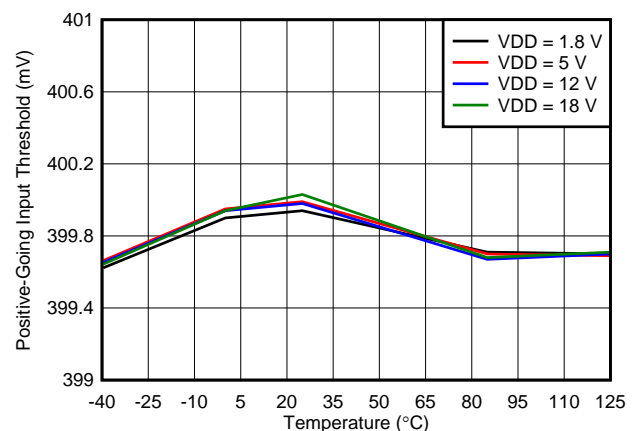
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS3710	SOT (6)	2.90 mm $\times$ 1.60 mm
	WSON (6)	1.50 mm $\times$ 1.50 mm

(1) For all available packages, see the package option addendum at the end of the datasheet.

#### Simplified Schematic



#### Rising Input Threshold Voltage ( $V_{IT+}$ ) vs Temperature



## Table of Contents

<b>1 Features</b> .....	<b>1</b>	7.4 Device Functional Modes.....	<b>10</b>
<b>2 Applications</b> .....	<b>1</b>	<b>8 Application and Implementation</b> .....	<b>11</b>
<b>3 Description</b> .....	<b>1</b>	8.1 Application Information.....	<b>11</b>
<b>4 Revision History</b> .....	<b>2</b>	8.2 Typical Application .....	<b>13</b>
<b>5 Pin Configuration and Functions</b> .....	<b>3</b>	8.3 Do's and Don'ts.....	<b>14</b>
<b>6 Specifications</b> .....	<b>4</b>	<b>9 Power-Supply Recommendations</b> .....	<b>15</b>
6.1 Absolute Maximum Ratings .....	<b>4</b>	<b>10 Layout</b> .....	<b>15</b>
6.2 ESD Ratings.....	<b>4</b>	10.1 Layout Guidelines .....	<b>15</b>
6.3 Recommended Operating Conditions.....	<b>4</b>	10.2 Layout Example .....	<b>15</b>
6.4 Thermal Information .....	<b>4</b>	<b>11 Device and Documentation Support</b> .....	<b>16</b>
6.5 Electrical Characteristics.....	<b>5</b>	11.1 Device Support.....	<b>16</b>
6.6 Timing Requirements .....	<b>6</b>	11.2 Documentation Support .....	<b>16</b>
6.7 Switching Characteristics .....	<b>6</b>	11.3 Community Resources.....	<b>16</b>
6.8 Typical Characteristics .....	<b>7</b>	11.4 Trademarks .....	<b>16</b>
<b>7 Detailed Description</b> .....	<b>9</b>	11.5 Electrostatic Discharge Caution.....	<b>16</b>
7.1 Overview .....	<b>9</b>	11.6 Glossary .....	<b>16</b>
7.2 Functional Block Diagram .....	<b>9</b>	<b>12 Mechanical, Packaging, and Orderable Information</b> .....	<b>16</b>
7.3 Feature Description.....	<b>10</b>		

## 4 Revision History

DATE	REVISION	NOTES
October 2015	*	Initial release

## 5 Pin Configuration and Functions



### Pin Functions

NAME	PIN		I/O	DESCRIPTION
	DDC	DSE		
GND	2, 4, 6	1, 3, 5	—	Connect all three pins to ground.
OUT	1	6	O	SENSE comparator open-drain output. OUT is driven low when the voltage at this comparator is below ( $V_{IT-}$ ). The output goes high when the sense voltage returns above the respective threshold ( $V_{IT+}$ ).
SENSE	3	4	I	This pin is connected to the voltage to be monitored with the use of an external resistor divider. When the voltage at this pin drops below the threshold voltage ( $V_{IT-}$ ), OUT is driven low.
VDD	5	2	I	Supply voltage input. Connect a 1.8-V to 18-V supply to VDD to power the device. Good analog design practice is to place a 0.1- $\mu$ F ceramic capacitor close to this pin.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

 over operating temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Voltage <sup>(2)</sup>	VDD	-0.3	20	V
	OUT	-0.3	20	
	SENSE	-0.3	7	
Current	OUT (output sink current)		40	mA
Temperature	Operating junction, T <sub>J</sub>	-40	125	°C
	Storage, T <sub>stg</sub>	-65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network ground pin.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	±2500
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	±1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>DD</sub>	Supply voltage	1.8		18	V
V <sub>I</sub>	Input voltage	0		6.5	V
V <sub>O</sub>	Output voltage	0		18	V

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS3710		UNIT
		DDC (SOT)	DSE (WSON)	
		6 PINS	6 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	204.6	194.9	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	50.5	128.9	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	54.3	153.8	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.8	11.9	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	52.8	157.4	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

Over the operating temperature range of  $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ , and  $1.8\text{ V} < V_{DD} < 18\text{ V}$  (unless otherwise noted). Typical values are at  $T_J = 25^\circ\text{C}$  and  $V_{DD} = 5\text{ V}$ .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(POR)}$	Power-on reset voltage <sup>(1)</sup>	$V_{OLmax} = 0.2\text{ V}$ , output sink current = $15\ \mu\text{A}$			0.8	V
$V_{IT+}$	Positive-going input threshold voltage	$V_{DD} = 1.8\text{ V}$	396	400	404	mV
		$V_{DD} = 18\text{ V}$	396	400	404	
$V_{IT-}$	Negative-going input threshold voltage	$V_{DD} = 1.8\text{ V}$	387	394.5	400	mV
		$V_{DD} = 18\text{ V}$	387	394.5	400	
$V_{hys}$	Hysteresis voltage ( $hys = V_{IT+} - V_{IT-}$ )			5.5	12	mV
$I_{(SENSE)}$	Input current (at the SENSE pin)	$V_{DD} = 1.8\text{ V}$ and $18\text{ V}$ , $V_I = 6.5\text{ V}$	-25	1	25	nA
$V_{OL}$	Low-level output voltage	$V_{DD} = 1.3\text{ V}$ , output sink current = $0.4\text{ mA}$			250	mV
		$V_{DD} = 1.8\text{ V}$ , output sink current = $3\text{ mA}$			250	
		$V_{DD} = 5\text{ V}$ , output sink current = $5\text{ mA}$			250	
$I_{lk(OD)}$	Open-drain output leakage-current	$V_{DD} = 1.8\text{ V}$ and $18\text{ V}$ , $V_O = V_{DD}$			300	nA
		$V_{DD} = 1.8\text{ V}$ , $V_O = 18\text{ V}$			300	
$I_{DD}$	Supply current	$V_{DD} = 1.8\text{ V}$ , no load		5.5	11	$\mu\text{A}$
		$V_{DD} = 5\text{ V}$		6	13	
		$V_{DD} = 12\text{ V}$		6	13	
		$V_{DD} = 18\text{ V}$		7	13	
UVLO	Undervoltage lockout <sup>(2)</sup>	$V_{DD}$ falling	1.3		1.7	V

(1) The lowest supply voltage ( $V_{DD}$ ) at which output is active;  $t_{r(VDD)} > 15\ \mu\text{s/V}$ . Below  $V_{(POR)}$ , the output cannot be determined.

(2) When  $V_{DD}$  falls below UVLO, OUT is driven low. The output cannot be determined below  $V_{(POR)}$ .

### 6.6 Timing Requirements

over operating temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$t_{pd(HL)}$	High-to-low propagation delay <sup>(1)</sup>		18		$\mu s$
$t_{pd(LH)}$	Low-to-high propagation delay <sup>(1)</sup>		29		$\mu s$
$t_{d(start)}$	Start-up delay <sup>(2)</sup>		150		$\mu s$

- (1) High-to-low and low-to-high refers to the transition at the input pin (SENSE).
- (2) During power on,  $V_{DD}$  must exceed 1.8 V for at least 150  $\mu s$  before the output is in a correct state.

### 6.7 Switching Characteristics

over operating temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_r$	Output rise time $V_{DD} = 5 V, 10\text{-mV}$ input overdrive, $R_P = 10 k\Omega, V_O = (0.1 \text{ to } 0.9) \times V_{DD}$		2.2		$\mu s$
$t_f$	Output fall time $V_{DD} = 5 V, 10\text{-mV}$ input overdrive, $R_P = 10 k\Omega, V_O = (0.1 \text{ to } 0.9) \times V_{DD}$		0.22		$\mu s$

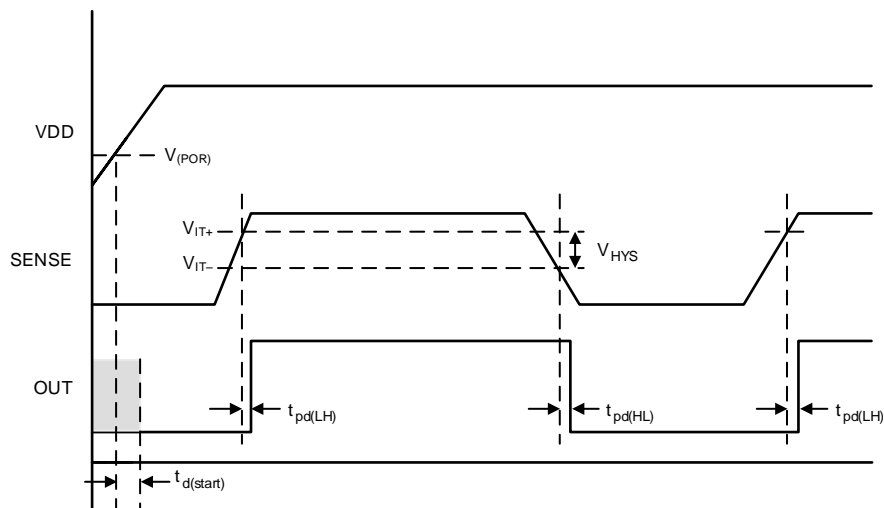


Figure 1. Timing Diagram

## 6.8 Typical Characteristics

at  $T_J = 25^\circ\text{C}$  and  $V_{DD} = 5\text{ V}$  (unless otherwise noted)

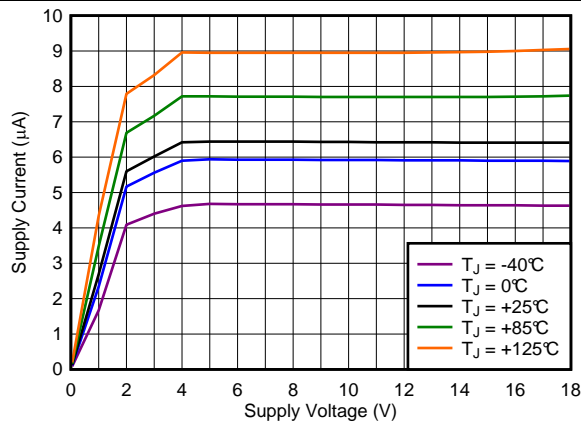


Figure 2. Supply Current ( $I_{DD}$ ) vs Supply Voltage ( $V_{DD}$ )

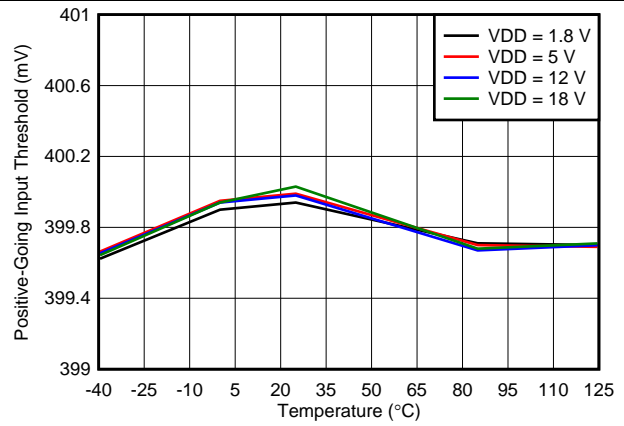


Figure 3. Rising Input Threshold Voltage ( $V_{IT+}$ ) vs Temperature

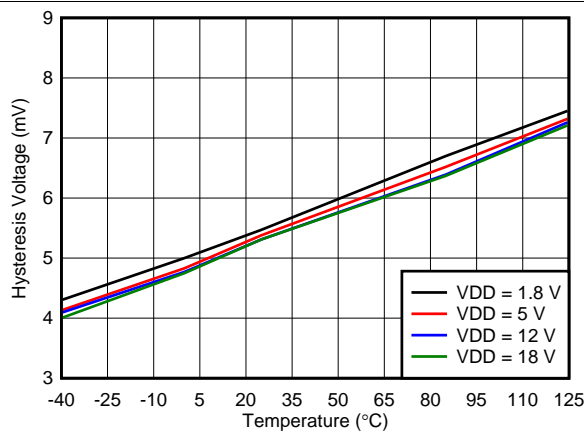


Figure 4. Hysteresis ( $V_{hys}$ ) vs Temperature

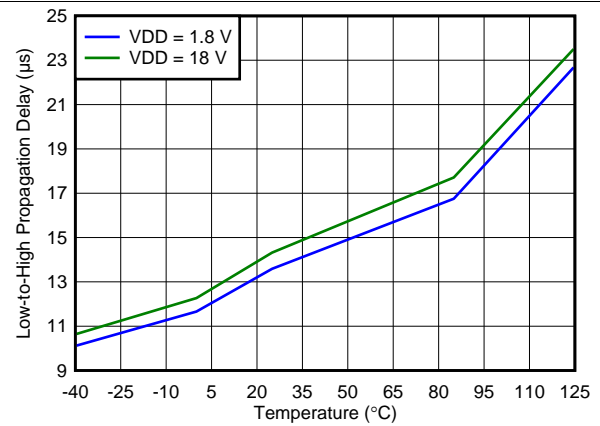


Figure 5. Propagation Delay vs Temperature (High-to-Low Transition at Sense)

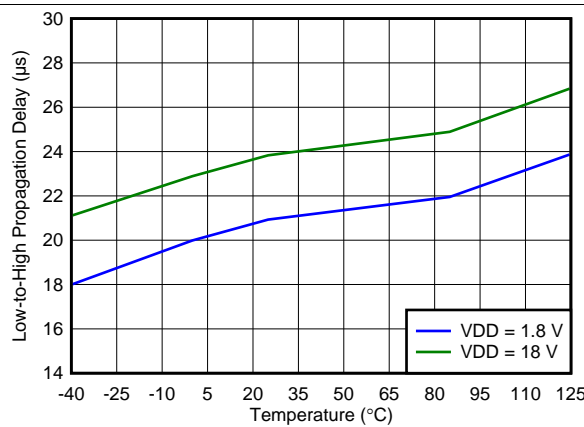


Figure 6. Propagation Delay vs Temperature (Low-to-High Transition at Sense)

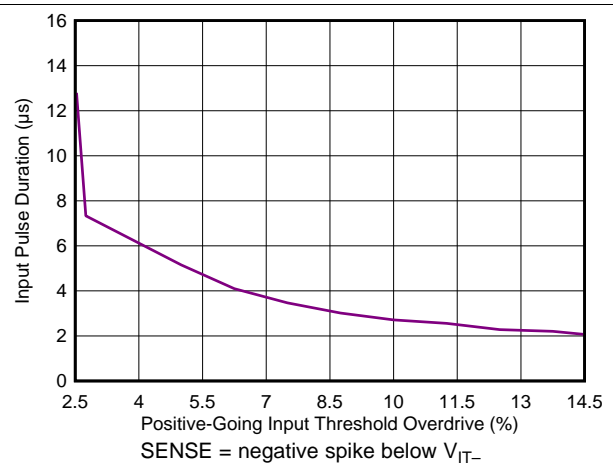


Figure 7. Minimum Pulse Width vs Threshold Overdrive Voltage  
SENSE = negative spike below  $V_{IT-}$

### Typical Characteristics (continued)

at  $T_J = 25^\circ\text{C}$  and  $V_{DD} = 5\text{ V}$  (unless otherwise noted)

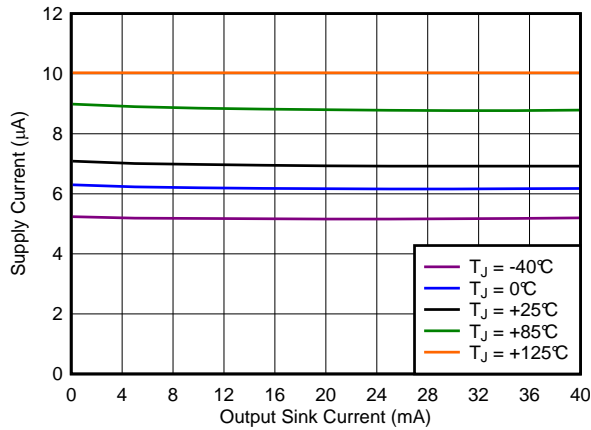


Figure 8. Supply Current ( $I_{DD}$ ) vs Output Sink Current

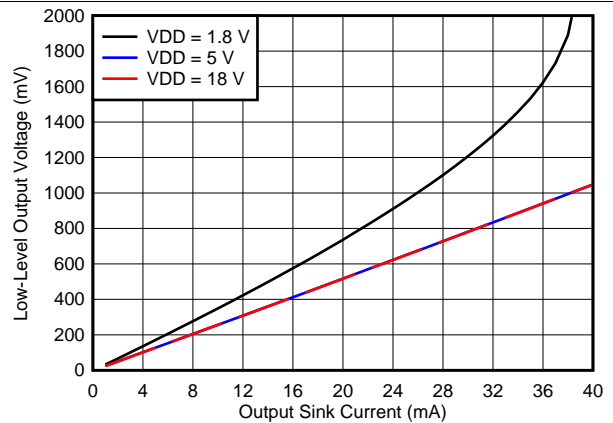


Figure 9. Output Voltage Low ( $V_{OL}$ ) vs Output Sink Current ( $-40^\circ\text{C}$ )

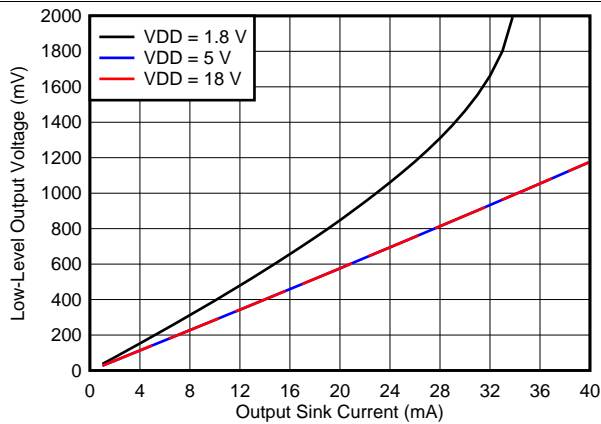


Figure 10. Output Voltage Low ( $V_{OL}$ ) vs Output Sink Current ( $0^\circ\text{C}$ )

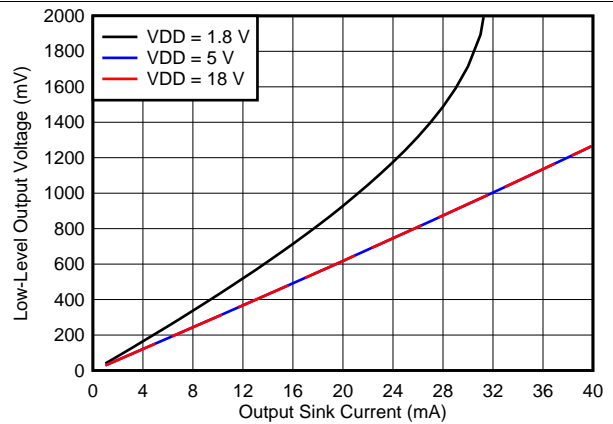


Figure 11. Output Voltage Low ( $V_{OL}$ ) vs Output Sink Current ( $25^\circ\text{C}$ )

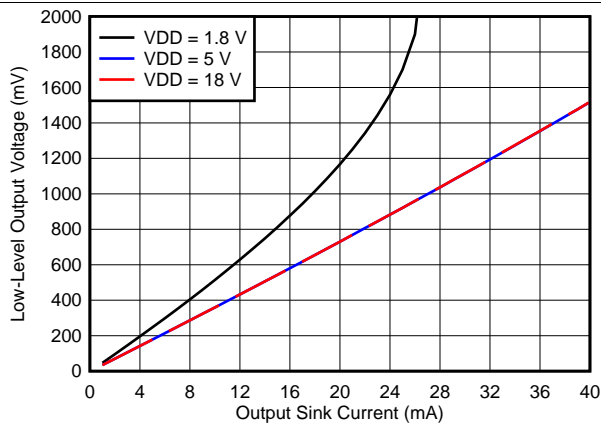


Figure 12. Output Voltage Low ( $V_{OL}$ ) vs Output Sink Current ( $85^\circ\text{C}$ )

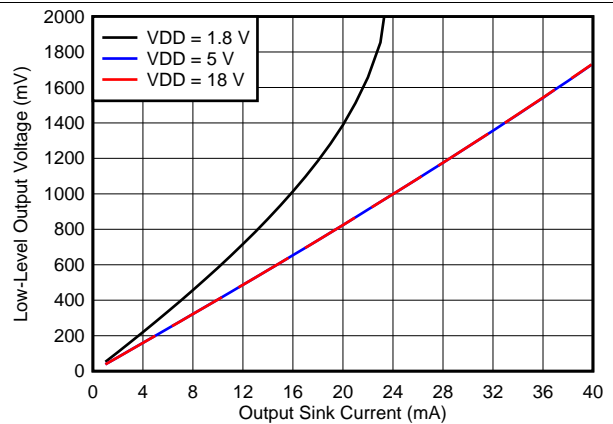


Figure 13. Output Voltage Low ( $V_{OL}$ ) vs Output Sink Current ( $125^\circ\text{C}$ )



## 7 Detailed Description

### 7.1 Overview

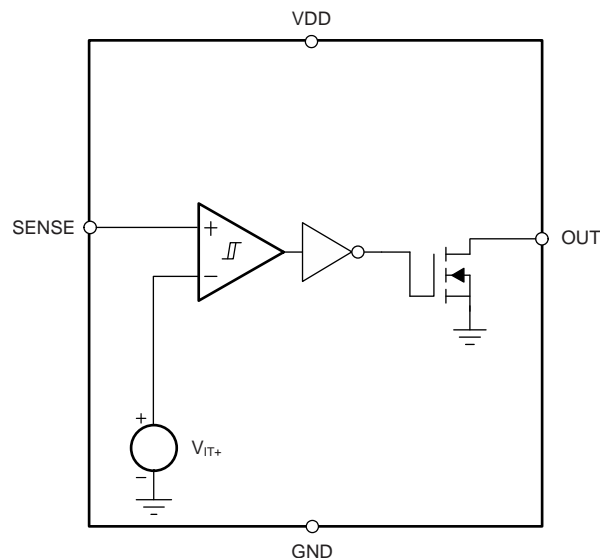
The TPS3710 provides precision voltage detection. The TPS3710 is a wide-supply voltage range (1.8 V to 18 V) device with a high-accuracy rising input threshold of 400 mV (1% over temperature) and built-in hysteresis. The output is also rated to 18 V, and can sink up to 40 mA.

The TPS3710 asserts the output signal, as shown in Table 1. To monitor any voltage above 0.4 V, set the input using an external resistor divider network. Broad voltage thresholds are supported that enable the device for use in a wide array of applications.

**Table 1. TPS3710 Truth Table**

CONDITION	OUTPUT	STATUS
$SENSE > V_{IT+}$	OUT high	Output not asserted
$SENSE < V_{IT-}$	OUT low	Output asserted

### 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 Input (SENSE)

The TPS3710 comparator has two inputs: one external input, and one input connected to the internal reference. The comparator rising threshold is trimmed to be equal to the reference voltage (400 mV). The comparator also has a built-in falling hysteresis that makes the device less sensitive to supply-rail noise and provides stable operation.

The comparator input (SENSE) is able to swing from ground to 6.5 V, regardless of the device supply voltage. Although not required in most cases, in order to reduce sensitivity to transients and layout parasitics for extremely noisy applications, place a 1-nF to 10-nF bypass capacitor at the comparator input.

OUT is driven to logic low when the input SENSE voltage drops below ( $V_{IT-}$ ). When the voltage exceeds  $V_{IT+}$ , the output (OUT) goes to a high-impedance state; see [Figure 1](#).

### 7.3.2 Output (OUT)

In a typical TPS3710 application, the output is connected to a reset or enable input of the processor (such as a digital signal processor [DSP], central processing unit [CPU], field-programmable gate array [FPGA], or application-specific integrated circuit [ASIC]) or the output is connected to the enable input of a voltage regulator (such as a dc-dc converter or low-dropout regulator [LDO]).

The TPS3710 device provides an open-drain output (OUT). Use a pullup resistor to hold this line high when the output goes to high impedance (not asserted). To connect the output to another device at the correct interface-voltage level, connect a pullup resistor to the proper voltage rail. The TPS3710 output can be pulled up to 18 V, independent of the device supply voltage.

[Table 1](#) and the [Input \(SENSE\)](#) section describe how the output is asserted or deasserted. See [Figure 1](#) for a timing diagram that describes the relationship between threshold voltage and the respective output.

### 7.3.3 Immunity to Input-Pin Voltage Transients

The TPS3710 is relatively immune to short voltage transient spikes on the sense pin. Sensitivity to transients depends on both transient duration and amplitude; see [Figure 7](#), *Minimum Pulse Width vs Threshold Overdrive Voltage*.

## 7.4 Device Functional Modes

### 7.4.1 Normal Operation ( $V_{DD} > UVLO$ )

When the voltage on  $V_{DD}$  is greater than 1.8 V for at least 150  $\mu$ s, the OUT signal correspond to the voltage on SENSE as listed in [Table 1](#).

### 7.4.2 Undervoltage Lockout ( $V_{(POR)} < V_{DD} < UVLO$ )

When the voltage on  $V_{DD}$  is less than the device UVLO voltage, and greater than the power-on reset voltage,  $V_{(POR)}$ , the OUT signal is asserted regardless of the voltage on SENSE.

### 7.4.3 Power-On Reset ( $V_{DD} < V_{(POR)}$ )

When the voltage on  $V_{DD}$  is lower than the required voltage to internally pull the asserted output to GND ( $V_{(POR)}$ ), SENSE is in a high-impedance state.

## 8 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The TPS3710 device is a wide-supply voltage comparator that operates over a  $V_{DD}$  range of 1.8 V to 18 V. The device has a high-accuracy comparator with an internal 400-mV reference and an open-drain output rated to 18 V for precision voltage detection. The device can be used as a voltage monitor. The monitored voltage are set with the use of external resistors.

#### 8.1.1 $V_{PULLUP}$ to a Voltage Other Than $V_{DD}$

The output is often tied to  $V_{DD}$  through a resistor. However, some applications may require the output to be pulled up to a higher or lower voltage than  $V_{DD}$  to correctly interface with the reset and enable pins of other devices.

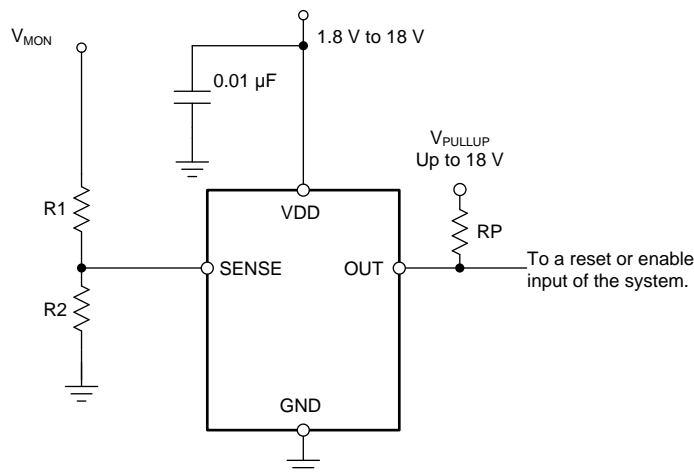
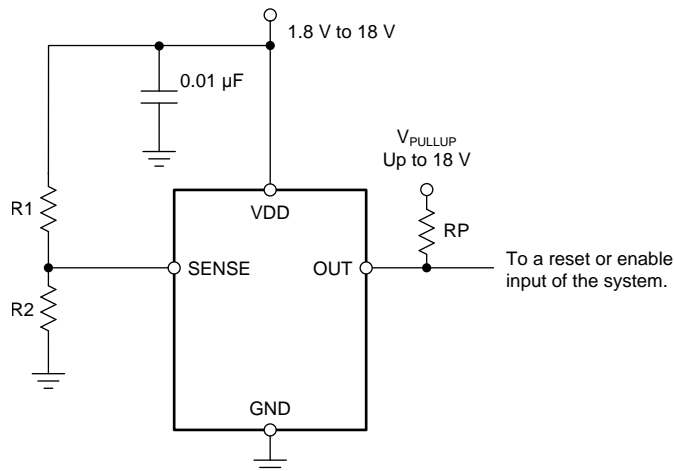


Figure 14. Interfacing to a Voltage Other Than  $V_{DD}$

## Application Information (continued)

### 8.1.2 Monitoring $V_{DD}$

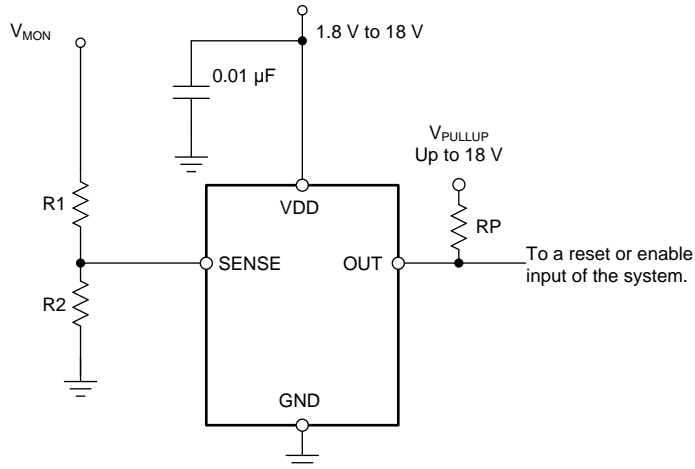
Many applications monitor the same rail that is powering  $V_{DD}$ . In these applications the resistor divider is simply connected to the  $V_{DD}$  rail.



**Figure 15. Monitoring the Same Voltage as  $V_{DD}$**

### 8.1.3 Monitoring a Voltage Other Than $V_{DD}$

Some applications monitor rails other than the one that is powering  $V_{DD}$ . In these types of applications the resistor divider used to set the desired threshold is connected to the rail that is being monitored.



NOTE: The input can monitor a voltage greater than maximum  $V_{DD}$  with the use of an external resistor divider network.

**Figure 16. Monitoring a Voltage Other Than  $V_{DD}$**

## 8.2 Typical Application

The TPS3710 device is a wide-supply voltage comparator that operates over a  $V_{DD}$  range of 1.8 to 18 V. The monitored voltage is set with the use of external resistors, so the device can be used either as a precision voltage monitor.

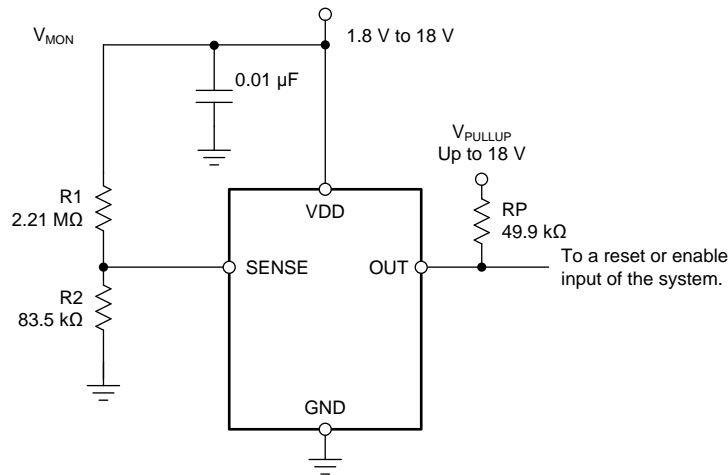


Figure 17. Wide VIN Voltage Monitor

### 8.2.1 Design Requirements

For this design example, use the values summarized in Table 2 as the input parameters.

Table 2. Design Parameters

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Monitored voltage	12-V nominal rail with maximum falling threshold of 10%	$V_{MON(UV)} = 10.99 \text{ V (8.33\%)}$

### 8.2.2 Detailed Design Procedure

#### 8.2.2.1 Resistor Divider Selection

The resistor divider values and target threshold voltage can be calculated by using Equation 1 to determine  $V_{MON(UV)}$ .

$$V_{MON(UV)} = \left( 1 + \frac{R1}{R2} \right) \times V_{IT-} \quad (1)$$

where

- R1 and R2 are the resistor values for the resistor divider on the SENSEx pins
- $V_{MON(UV)}$  is the target voltage at which an undervoltage condition is detected

Choose  $R_{TOTAL}$  ( $= R1 + R2$ ) so that the current through the divider is approximately 100 times higher than the input current at the SENSE pin. The resistors can have high values to minimize current consumption as a result of low input bias current without adding significant error to the resistive divider. For details on sizing input resistors, refer to application report [SLVA450, Optimizing Resistor Dividers at a Comparator Input](#), available for download from [www.ti.com](http://www.ti.com).

### 8.2.2.2 Pullup Resistor Selection

To ensure the proper voltage level, the pullup resistor value is selected by ensuring that the pullup voltage divided by the resistor does not exceed the sink-current capability of the device. This confirmation is calculated by verifying that the pullup voltage minus the output-leakage current ( $I_{lkg(OD)}$ ) multiplied by the resistor is greater than the desired logic-high voltage. These values are specified in the [Electrical Characteristics](#).

Use [Equation 2](#) to calculate the value of the pullup resistor.

$$\frac{(V_{HI} - V_{PU})}{I_{lkg(OD)}} \geq R_{PU} \geq \frac{V_{PU}}{I_O} \quad (2)$$

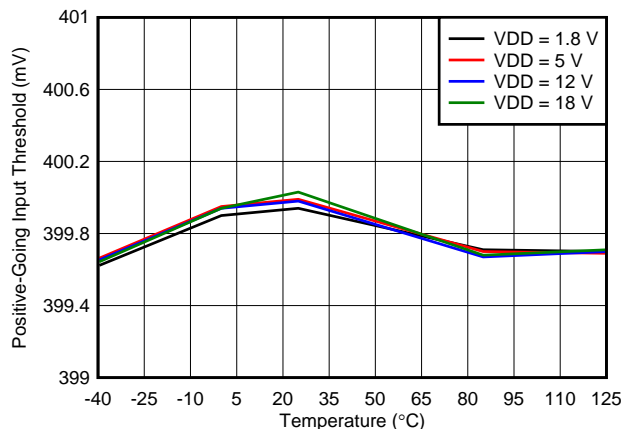
### 8.2.2.3 Input Supply Capacitor

Although an input capacitor is not required for stability, for good analog design practice, connect a 0.1- $\mu$ F low equivalent series resistance (ESR) capacitor across the VDD and GND pins. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is not located close to the power source.

### 8.2.2.4 Sense Capacitor

Although not required in most cases, for extremely noisy applications, place a 1-nF to 10-nF bypass capacitor from the comparator input (SENSE) to the GND pin for good analog design practice. This capacitor placement reduces device sensitivity to transients.

## 8.2.3 Application Curves



**Figure 18. Rising Input Threshold Voltage ( $V_{IT+}$ ) vs Temperature**

## 8.3 Do's and Don'ts

Do connect a 0.1- $\mu$ F decoupling capacitor from  $V_{DD}$  to GND for best system performance.

If the monitored rail is noisy, do connect a decoupling capacitor from the comparator input (sense) to GND.

Don't use resistors for the voltage divider that cause the current through them to be less than 100 times the input current of the comparator without also accounting for the effect to the accuracy.

Don't use a pullup resistor that is too small, because the larger current sunk by the output then exceeds the desired low-level output voltage ( $V_{OL}$ ).

## 9 Power-Supply Recommendations

These devices operate from an input voltage supply range between 1.8 V and 18 V.

## 10 Layout

### 10.1 Layout Guidelines

Placing a 0.1- $\mu\text{F}$  capacitor close to the VDD pin to reduce the input impedance to the device is good analog design practice.

### 10.2 Layout Example

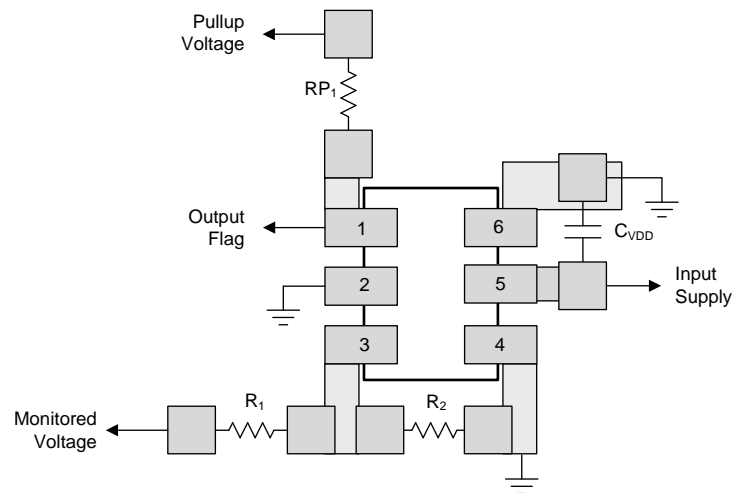


Figure 19. Layout Example

## 11 Device and Documentation Support

### 11.1 Device Support

#### 11.1.1 Device Nomenclature

**Table 3. Device Nomenclature**

PRODUCT	DESCRIPTION
TPS3710yyyz	yyy is package designator z is package quantity

### 11.2 Documentation Support

#### 11.2.1 Related Documentation

For related documentation, see the following:

- *Optimizing Resistor Dividers at a Comparator Input*, [SLVA450](#)

### 11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.4 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 11.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3710DDCR	ACTIVE	SOT-23-THIN	DDC	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11AO	<a href="#">Samples</a>
TPS3710DDCT	ACTIVE	SOT-23-THIN	DDC	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	11AO	<a href="#">Samples</a>
TPS3710DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	1A	<a href="#">Samples</a>
TPS3710DSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	1A	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3710DDCR	SOT-23-THIN	DDC	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3710DDCT	SOT-23-THIN	DDC	6	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3710DSER	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TPS3710DSET	WSON	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2

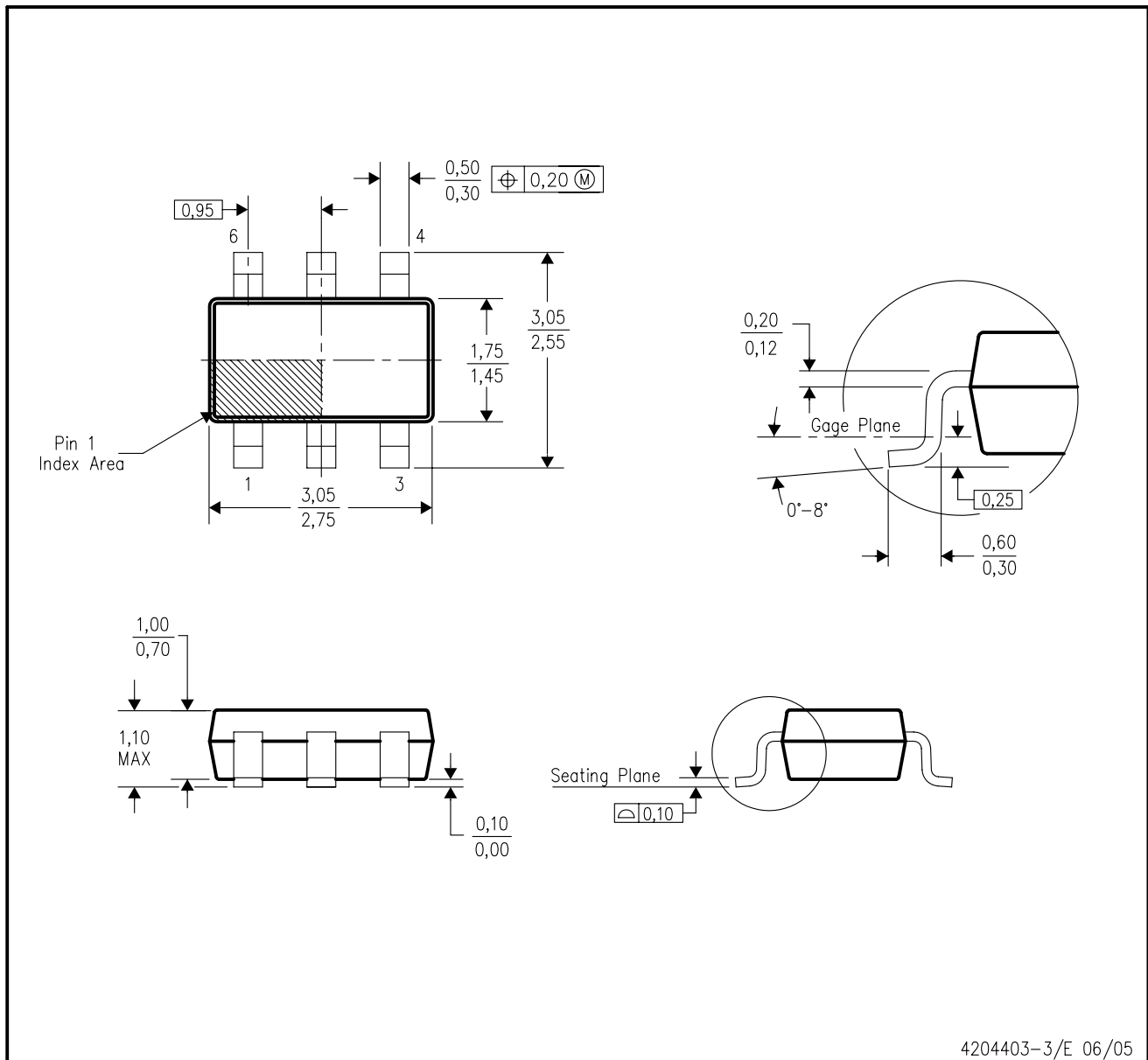
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3710DDCR	SOT-23-THIN	DDC	6	3000	195.0	200.0	45.0
TPS3710DDCT	SOT-23-THIN	DDC	6	250	195.0	200.0	45.0
TPS3710DSER	WSON	DSE	6	3000	203.0	203.0	35.0
TPS3710DSET	WSON	DSE	6	250	203.0	203.0	35.0

DDC (R-PDSO-G6)

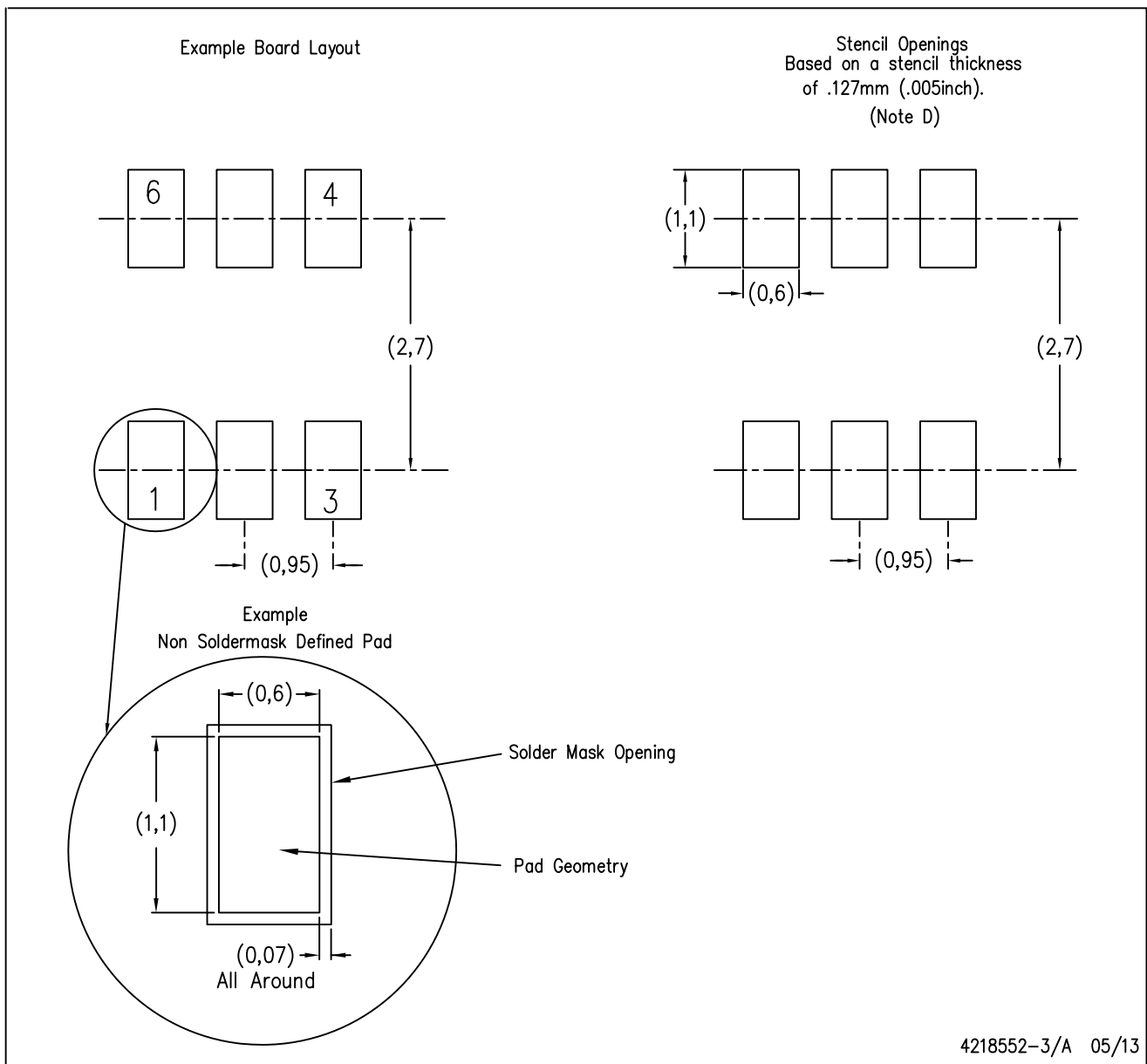
PLASTIC SMALL-OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion.
  - Falls within JEDEC MO-193 variation AA (6 pin).

DDC (R-PDSO-G6)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DSE (S-PDSO-N6)

PLASTIC SMALL OUTLINE



4207810/A 03/06

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Small Outline No-Lead (SON) package configuration.
  - D. This package is lead-free.

## IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.